AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jeon, et al.**	Art Unit: 2814
Serial No.: 10/761,009	Examiner: Pham, Long
Filed: 01/20/2004	
For: **Method for Forming a Thin, High Quality Buffer Layer in a Field Effect Transistor and Related Structure**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-2, 4-6, 8-9, and 11-13. The Final Rejection issued on July 26, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on October 26, 2005.

01/11/2006 TBESHAH1 00000017 10761009
01 FC:1402 500.00 OP

01/11/2006 TBESHAH1 00000017 10761009
02 FC:1251 120.00 OP

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-2, 4-6, 8-9, and 11-13 are pending, and claims 3, 7, 10, and 14-20 were canceled in previous amendments. Claims 1-2, 4-6, 8-9, and 11-13 have been finally rejected in a Final Rejection dated July 26, 2005. This Appeal is directed to the rejection of claims 1-2, 4-6, 8-9, and 11-13 which appear in the attached "Appendix of Claims on Appeal."

STATUS OF AMENDMENTS

No claim amendments have been entered after issuance of the Final Rejection of July 26, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1

Independent claim 1 defines a method for forming a field-effect transistor (e.g., field-effect transistor 202 in Figure 2) on a substrate (e.g., substrate 204 in Figure 2). The method includes a step of using a silicon tetrachloride ("$SiCl_4$") precursor in an atomic layer deposition ("ALD") process to form a buffer layer (e.g., ALD buffer layer 212 in Figure 2) on the substrate. Thereafter, a high-k dielectric layer (e.g., high-k dielectric layer 214 in Figure 2) is formed over the ALD buffer layer. The high-K dielectric layer can be made of aluminum oxide, hafnium oxide, or zirconium oxide.

Claim 2

Claim 2 depends from claim 1 and claims a subsequent step of forming a gate electrode layer (e.g., gate electrode layer 216 in Figure 2) over the high-k dielectric layer. Claim 2 thus clarifies that the ALD buffer layer is utilized in the gate of the field-effect transistor.

Claim 8

Independent claim 8 defines a method substantially similar to that defined by independent claim 1.

Claim 9

Dependent claim 9 defines a method substantially similar to that defined by dependent claim 2.

GROUND(S) OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 4-6, 8, and 11-13 under 35 USC §103(a) as being unpatentable over U.S. Patent No. 6,563,183 to En et al (hereinafter "En") in combination with U.S. Patent Publication No. 2005/0048765 to Kim (hereinafter "Kim").

B. Claims 2 and 9 under 35 USC §103(a) as being unpatentable over En in combination with Kim.

ARGUMENT

A. Rejection of claims 1, 4-6, 8, and 11-13 under 35 USC §103(a) as being unpatentable over En in combination with Kim.

Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 8, is patentably distinguishable over En and Kim, either singly or in combination.

En is directed to a gate array with multiple dielectric properties. According to En, an integrated circuit is fabricated on a semiconductor substrate, including first and second field effect transistors. The first field effect transistor includes a first polysilicon gate positioned above a first channel region of the substrate and isolated from the first channel

region by a first dielectric layer extending the entire length of the first polysilicon gate. The first dielectric layer includes a first dielectric material with a first dielectric constant. The second field effect transistor consists of a second polysilicon gate positioned above a second channel region on the substrate and isolated from the second channel region by a second dielectric layer extending the entire length of the second polysilicon gate. The second dielectric layer has a second dielectric material with a second dielectric constant. The first dielectric constant and the second dielectric constant may be different. *See* the flow chart of Figure 2, and Figures 5a through 5i and their related descriptions in En.

According to En, utilization of different dielectrics with different dielectric constants results in a gate array that can include smaller, faster transistors having a high dielectric constant, with additional flexibility in that transistors with different operating properties can be fabricated and used. *See*, column 10, lines 13-21 of En.

However, En is not directed to formation of a thin, high quality buffer layer utilizing a silicon tetrachloride precursor in a field effect transistor in order to prevent the problems associated with transistor gates having low quality, non-uniform, thick, lower-k, and pin-holed dielectrics which in turn result from randomly and unintendedly grown thermal oxide at the silicon/high k interface in the gate of the transistor. *See*, for example, page 8, line 20 through page 9, line 9 of the present application. Moreover, the present invention teaches use of aluminum oxide, which is specifically suitable for use as a high-k dielectric over an ALD silicon oxide layer and in the gate of a transistor.

Thus, the present invention discloses and claims "utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form a buffer layer" on the substrate and "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer comprising aluminum oxide." In addition to the fact that En does not address the problems addressed by the present invention, En does not disclose or suggest, for example, use of silicon tetrachloride precursor, nor use of aluminum oxide as a high-k dielectric. Moreover, En does not disclose or suggest use of an ALD silicon oxide buffer layer formed with silicon tetrachloride precursor and an overlying high-k dielectric layer formed with aluminum oxide. As such, the present invention, as defined by the amended claims, is patentably distinguishable over En.

The Examiner has cited Kim as disclosing use of silicon tetrachloride to form oxide in an ALD process. However, Kim is directed to sealing pores in a *low-k dielectric* damascene process for forming conductive layers. See, for example, Figure 3A of Kim and its related description. As such, Kim specifically teaches away from use of an ALD layer in conjunction with *high-k dielectrics*. For example, Kim does not disclose or suggest "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer comprising aluminum oxide." Moreover, Kim is not directed to fabrication of a field effect transistor, but to the formation of conductive patterns in a damascene process.

The Examiner has stated that Kim is cited for suggesting that an ALD layer formed with silicon tetrachloride precursor can be used in a transistor utilizing a high-k gate dielectric. However, there is no suggestion whatsoever in Kim for such a departure from

the teachings of Kim, where Kim in fact discloses sealing pores in a *low-k dielectric* damascene process. It is noted that Applicant has not claimed that the invention has for the first time utilized an ALD layer, nor that the invention has for the first time utilized a high-k dielectric. Likewise, Applicant has not claimed that the invention is about forming an ALD layer with silicon tetrachloride precursor. Applicant has merely claimed that the combination of an ALD buffer layer formed with silicon tetrachloride precursor, and a high-k dielectric formed with aluminum oxide, both in a field effect transistor, is novel and inventive. It is submitted that Kim does not provide suggestions or teachings to cure the deficiencies of En. In other words, the general proposition that an ALD layer can be formed with silicon tetrachloride precursor does not suggest or overcome the deficiencies of En discussed above.

B. Rejection of claims 2 and 9 under 35 USC §103(a) as being unpatentable over En in combination with Kim.

Applicant submits that, at a minimum, the invention defined by dependent claims 2 and 9 is patentably distinguishable over En and Kim, either singly or in combination.

As discussed above, En is not directed to formation of a thin, high quality buffer layer utilizing a silicon tetrachloride precursor in a field effect transistor in order to prevent the problems associated with *transistor gates* having low quality, non-uniform, thick, lower-k, and pin-holed dielectrics which in turn result from randomly and unintendedly grown thermal oxide at the silicon/high k interface in *the gate* of the

transistor. *See*, for example, page 8, line 20 through page 9, line 9 of the present application. However, the invention defined by dependent claims 2 and 9 claims use of aluminum oxide, which is specifically suitable for use as a high-k dielectric over an ALD silicon oxide layer and in the *gate of a transistor*.

Dependent claims 2 and 9 require "forming a gate electrode layer over [the] high-k dielectric layer." In addition to the fact that En does not address the problems addressed by the present invention, En does not disclose or suggest, for example, use of silicon tetrachloride precursor, nor use of aluminum oxide as a high-k dielectric. Moreover, En does not disclose or suggest use of an ALD silicon oxide buffer layer formed with silicon tetrachloride precursor and an overlying high-k dielectric layer formed with aluminum oxide as parts of a *gate of a transistor*. As such, the present invention, as defined by dependent claims 2 and 9, is patentably distinguishable over En.

Moreover, as discussed above, Kim is directed to sealing pores in a *low-k dielectric* damascene process for forming conductive layers. As such, Kim specifically teaches away from use of an ALD layer in conjunction with *high-k dielectrics*. For example, Kim does not disclose or suggest "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer comprising aluminum oxide." Further, Kim is not directed to fabrication of a field effect transistor or *its gate*, but to the formation of conductive patterns in a damascene process. In contrast, dependent claims 2 and 9 claim "forming a gate electrode layer over [the] high-k dielectric layer."

Kim is not directed to formation of *transistor gates*, but to patterning conductors. In sum, claims 2 and 9 claim that the combination of an ALD buffer layer formed with silicon tetrachloride precursor, and a high-k dielectric formed with aluminum oxide, both *in the gate of* a field effect transistor, is novel and inventive. It is submitted that Kim does not provide suggestions or teachings to cure the deficiencies of En. In other words, the general proposition that an ALD layer can be formed with silicon tetrachloride precursor does not suggest or overcome the deficiencies of En discussed above.

CONCLUSION

For all the foregoing reasons, Applicant respectfully submits that independent claims 1 and 8 are patentably distinguishable over En and Kim, either singly or in combination. Therefore, dependent claims 4-6 and 11-13 are also patentably distinguishable over En and Kim for reasons similar to those discussed above, and further for the additional limitations contained in each dependent claim. Moreover, dependent claims 2 and 9 are allowable for the additional reasons separately discussed in relation to dependent claims 2 and 9. Thus, an early allowance of claims 1-2, 4-6, 8-9, and 11-13 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 1/6/06

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Date of Deposit: Jan. 6, 2006.

LESLEY L. NING
Name of Person Mailing Paper and/or Fee

Signature 1/6/06
Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A method of forming a field-effect transistor on a substrate, said method comprising steps of:

utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form a buffer layer on said substrate;

forming a high-k dielectric layer over said buffer layer, said high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

Claim 2: The method of claim 1 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 4: The method of claim 1 wherein said buffer layer comprises substantially no pin-hole defects.

Claim 5: The method of claim 1 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 6: The method of claim 2 wherein said gate electrode layer comprises polycrystalline silicon.

Claim 8: A method for forming a field effect transistor on a substrate, said method comprising a step of forming a buffer layer on said substrate, said method being characterized by:

utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form said buffer layer on said substrate;

forming a high-k dielectric layer on said buffer layer, said high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

Claim 9: The method of claim 8 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 11: The method of claim 8 wherein said buffer layer comprises substantially no pin-hole defects.

Claim 12: The method of claim 8 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 13: The method of claim 9 wherein said gate electrode layer comprises polycrystalline silicon.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/8/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT | **$620.00**

Complete if Known	
Application Number	10/761,009
Filing Date	01/20/2004
First Named Inventor	Jeon
Examiner Name	Pham, Long
Art Unit	2814
Attorney Docket No.	0180154

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: **50-0731** Deposit Account Name: **Farjami & Farjami LLP**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 20 or HP =	0	x	$50.00	=	$ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 3 or HP =	0	x	$200.00	=	$ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
$360.00	

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
	- 100 =	0	/ 50 =	0	(round up to a whole number) x	$250.00	=	$ 0.00

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: **Filing a brief in support of an appeal and One Month Extension (37 CFR §1.136)**	**$620.00**

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 38135	Telephone (949) 282-1000
Name (Print/Type)	Michael Farjami, Esq.		Date 1/6/06